In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) An apparatus, comprising:

a processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

an event selection control register (ESCR ~~ECSR~~) coupled to the processor;

a first multiplexer coupled to the ESCR ~~ECSR~~ to select a class of events, based on a first set of control signals from the ESCR ~~ECSR~~, from a group of event signals issued from the processor;

a second multiplexer coupled to the ESCR ~~ECSR~~ and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

a logic circuit coupled to the ESCR and the second multiplexer to qualify the event based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred; and

an event counter to count the event qualified by the logic circuit.

2. (Cancelled)

3. (Previously Presented) The apparatus of claim 1, wherein the ESCR comprises a first field of bits to store the first set of control signals to select the class of events.

4. (Previously Presented) The apparatus of claim 3, wherein the ESCR further comprises a second field of bits to store the second set of control signals to mask the subclasses.

5-6. (Cancelled)

7. (Previously Presented) The apparatus of claim 1, wherein the event counter is stopped and cleared before a new event is selected.

8. (Previously Presented) The apparatus of claim 7, wherein the event counter is preset to a certain state.

9. (Previously Presented) The apparatus of claim 1, wherein the class of events includes hardware performance and breakpoint events.

10-17. (Cancelled)

18. (Currently Amended) A method, comprising:

executing a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

instructing a first multiplexer, based on a first set of signals from an event selection control register (ESCR ~~ECSR~~), to select a class of events from a group of event signals issued from the processor;

instructing a second multiplexer, based on a second set of signals from the ESCR ~~ECSR~~, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

qualifying the event, by a logic circuit, based on a thread ID and a thread CPL, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred;

counting the event qualified by the logic circuit using an event counter; and

accessing the event counter to determine a current count of the event.

19. (Cancelled)

20. (Previously Presented) The method in claim 18, wherein the qualifying the event includes requiring that the event has a preselected thread ID.

21. (Previously Presented) The method in claim 20, wherein the qualifying the event further includes requiring that the event has a preselected thread CPL.

22-26. (Cancelled)

27. (Previously Presented) The method of claim 18, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

28. (Previously Presented) The method of claim 20, wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred.

29. (Previously Presented) The method of claim 21, wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred.

30. (Previously Presented) The apparatus of claim 1, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

31. (Previously Presented) The apparatus of claim 1, further comprising an access location to allow access to the event counter to determine a current count of the event.

32. (Previously Presented) A system, comprising:

a storage medium coupled with a processor, the processor to execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

an event selection control register (ESCR) coupled to the processor; a first multiplexer coupled to the ESCR to select a class of events, based on a first set of control signals from the ESCR, from a group of event signals issued from the processor;

a second multiplexer coupled to the ESCR and the first multiplexer to mask, based on a second set of control signals from the ESCR, subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

a logic circuit coupled to the ESCR and the second multiplexer to qualify the event that is to be selected based on a thread ID and a thread current privilege level (CPL), the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred;

an event counter to count the event qualified by the logic circuit; and

an access location to allow access to the event counter to determine a current count of the event.

33. (Previously Presented) The system of claim 32, wherein the access location allows access to determine the count without disturbing the operation of event counter.

34. (Previously Presented) The system of claim 33, wherein the ESCR comprises a first field of bits to store the first set of control signals to select the class of events.

35. (Previously Presented) The system of claim 34, wherein the ESCR further comprises a second field of bits to store the second set of control signals to mask the subclasses.

36. (Previously Presented) The system of claim 32, wherein the event counter is stopped and cleared before a new event is selected.

37. (Previously Presented) The system of claim 36, wherein the event counter is preset to a certain state.

38. (Previously Presented) The system of claim 32, wherein the class of events includes hardware performance and breakpoint events.

39. (Previously Presented) The system of claim 32, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

40. (Previously Presented) A machine-readable medium having stored thereon data representing sets of instructions, the sets of instructions which, when executed by a machine, cause the machine to:

execute a plurality of threads simultaneously, each thread including a series of instructions and resulting in an event;

instruct a first multiplexer, based on a first set of signals from an event selection control register (ESCR), to select a class of events from a group of event signals issued from the processor;

instruct a second multiplexer, based on a second set of control signals from the ESCR, to mask subclasses of the class of events in order to select an event that belongs to a subclass that is not masked;

qualify the event, by a logic circuit, based on a thread ID and a thread CPL, the thread ID indicating a source of the event including a thread of the plurality of threads where the event occurred;

count the event qualified by the logic circuit using an event counter; and

access the event counter to determine a current count of the event.

41. (Previously Presented) The machine-readable medium of claim 40, wherein to qualify the event includes requiring that the event has a preselected thread ID.

42. (Previously Presented) The machine-readable medium in claim 41, wherein to qualify the event further includes requiring that the event has a preselected thread CPL.

43. (Previously Presented) The machine-readable medium of claim 40, wherein the thread CPL indicates a privilege level at which the thread at which the event occurred was operating when the event occurred.

44. (Previously Presented) The machine-readable medium of claim 40, wherein the preselected thread ID represents a thread of the plurality of threads where the event occurred.

45. (Previously Presented) The machine-readable medium of claim 41, wherein thread CPL indicates a privilege level at which the thread was operating at when the event occurred.